

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

## Patent Application Transmittal

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Sir:

Transmitted herewith for filing is the patent application of

Inventors: **R. Dean Adams, Thomas J. Eckenrode, Steven L. Gregor, Kamran Zarrineh**For: **SYSTEM INITIALIZATION OF MICROCODE-BASED MEMORY BUILT-IN SELF-TEST**

Enclosed are:

3 sheets of informal drawings consisting of 5 figures.  
 An assignment of the invention to: International Business Machines Corporation, Armonk, New York 10504  
 A certified copy of application Serial No.:  
 An Information Disclosure Statement.  
 A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 and 1.27.  
 A combined declaration and power of attorney (unsigned).  
 A preliminary amendment.

The filing fee has been calculated as shown below:

(Col. 1)	(Col. 2)
For:	No. Filed
Basic Fee	
Total Claims	17 - 20 =
Indep. Claims	3 - 3 =
Multiple Dependent Claim Presented	

Other Than Small Entity	
Rate	Fee
	\$ 690.00
0 x \$18.00 =	\$ 0.00
0 x \$78.00 =	\$ 0.00
\$260.00	\$ 0.00
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Respectfully submitted,

FOR: **R. Dean Adams, Thomas J. Eckenrode, Steven L. Gregor, Kamran Zarrineh**

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CERTIFICATE OF MAILING UNDER 37 CFR 1.10	
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SYSTEM INITIALIZATION OF MICROCODE-BASED  
MEMORY BUILT-IN SELF-TEST

DESCRIPTION

BACKGROUND OF THE INVENTION

5

Field of the Invention

10

The present invention generally relates to testing of integrated circuit devices including memory structures and systems including such integrated circuits and, more particularly, to extending built-in self-test (BIST) arrangements to systems testing.

15

Increases in integration density of integrated circuits has greatly increased the performance and functionality of the circuits which can be included on a single semiconductor chip. Increased functionality, of course, requires increased circuit complexity and, at the present state of the art, many functionally differentiated regions such as adders, processors, logic arrays, buffers, decoders level converters and the like may be included on a single chip. These functionally differentiated regions are often designed to operate at different clock rates and even different voltages while being required to communicate with each other in a generally synchronized fashion.

Design of storage devices and processes for their fabrication have become quite sophisticated and has resulted in very low process cost for fabrication and very small memory cell area.

5 Therefore it is currently practical to form even relatively large numbers of storage cells together with digital signal processing circuitry on a single chip. Moreover, use of multi-port memories for communication between functional components on a  
10 chip has proven to be extremely fast and efficient and thus has come into relatively widespread use. These memories are generally referred to as embedded memories when included with circuits having other than a storage function on an integrated circuit chip.

15 Nevertheless, memory cells, particularly of the dynamic type which store data capacitively, are relatively delicate devices and may be subject to damage or deterioration during manufacture or after  
20 being placed in service. When such devices are used for communication and data transfer among functional regions or components, the reliability of storage devices becomes extremely critical to the proper operation of the entire chip. Therefore, it is  
25 desirable to test storage cells at different stages of manufacture, board assembly and during system operation. This test is done periodically or at certain system operating states such as power-up of the chip in order to ascertain operability of the  
30 memory structures. It is also desirable to provide for broader testing of the various functional elements of the system operating together. Such

tests are generally referred to as system level tests but cannot generally be performed by programmable memory BIST arrangements as will be discussed below.

5 Nevertheless, system failures may be attributed to damage caused by external elements, minor manufacturing imperfections and/or aging of the materials. Damage from external elements could impact the correct functioning of an electronic  
10 system or any part thereof at any time during its useable life. However, minor manufacturing imperfections are the main cause of system failures at early stages of system operation while aging is is the dominant cause of system failures at later  
15 stages of the life time of the system. For high reliability and availability applications such as banking and medical applications, it is essential to perform periodic testing of system modules.

20 Memory devices are usually in the critical path of a system or its respective components and therefore their design is directed to ensure that memories in critical paths operate several times faster than their surrounding logic which is realized through aggressive design utilizing dense  
25 fabrication and new technologies. These factors may make embedded memories somewhat more prone to failures due to minor manufacturing imperfections and aging and thus must be tested periodically after being placed in service in addition to manufacturing  
30 level and board level testing.

Further, system level tests could be performed by dedicated hardware, independent of that used for

manufacturing level and board level tests. However, in such a case, the hardware dedicated to manufacturing level and board level testing which is generally provided as a built-in self-test 5 arrangement would have no function after the system is placed in service while the additional hardware provided for system level testing would increase the hardware overhead for testing of all types.

However, access to embedded memories for 10 testing is often difficult, particularly where chip space and external connections are at a premium. For that reason, it is preferred to form a self-test circuit on the chip, itself. Numerous types of such arrangements are known and generally referred to as 15 a built-in self-test (BIST) circuit or engine. Some forms of BIST circuits have been developed which allow the test sequence to be dynamically modified based on results of test procedures in order to accelerate the testing process. The amount of chip 20 space which can be efficiently allocated to a BIST arrangement is very limited, generally to about 2% of the area of the storage devices to be tested.

This area must also include space for an 25 instruction or signal source, such as a read-only-memory (ROM) and, usually, a decoder, to generate the coded digital signals with which the embedded memory is to be exercised during the self-test operation. At the present state of the art, maintaining the BIST arrangement within such a chip 30 area constraint presents a major challenge, particularly where the memory structure is complex and extended numbers of sequences of signals are

required to adequately test the memory and/or to capture signals from the memory for evaluation in the course of the self-test.

Even when the chip area is limited to a small percentage of the area of the memory to be tested, the chip space is considered to be inefficiently used since the BIST arrangement is not used in the other intended functions of the chip. Nevertheless, the use of a BIST arrangement may be the only practical technique for accessing the signal lines necessary for testing of an embedded memory. Accordingly, BIST architectures, including programmable memory BIST architectures which can alter the test procedure in response to test results, have been developed. Programmable BIST architectures also can accommodate different memory test signal patterns that may be required for different memory structures without significant hardware modification and associated design costs.

A programmable memory BIST arrangement often includes a programmable memory BIST controller and other components to generate the signals necessary to fully exercise and test the particular memory structure of interest. The programmable memory BIST controller generally includes a microcode-based controller and an instruction decode module which will develop one or more multi-bit signals (e.g. multi-bit data, address and control signals) for each instruction.

The instructions supported by the programmable memory BIST controller describe or constitute a memory test algorithm appropriate to the particular

embedded memory to be tested and are stored in an instruction store module, preferably (or conceptually) within the microcode based controller. The instruction store module may be of any of a variety of forms including but not limited to a read only memory (ROM) such as an EEPROM or a register file. In the former case (e.g. where storage is non-volatile) no loading of the test instructions is necessary and may not be possible. Also, ROM and small RAM modules complicate the overall testing of the system.

Therefore, the use of a register file for storage of test instructions is generally preferred. In this case, the instructions for a particular desired test are loaded during the test process by means of an external tester. (It should be appreciated that while an external tester may be required for conducting a test procedure, the BIST may provide access to particular connections in the memory structures which are impractical to access otherwise.)

In a manufacturing level test (e.g. during chip manufacture and packaging) the supported instructions representing the test algorithm are input from an external tester as described above. If the storage elements in the register file are scannable, the loading process is performed serially using any scan protocol which has been adopted and/or which may be convenient. In board level testing in accordance with the IEEE 1149.1 standard, the register file is defined as a test data register and is accessed by loading an appropriate IEEE

1149.1 instruction in the instruction register. The memory test instructions are loaded using an external tester while the test access port (TAP) controller is in the SHIFT-DR state.

5        However, the BIST modules that use register files as their instruction store module cannot be used for system level tests. This is due to the fact that register files need to be initialized to the instruction set representing the test algorithm.

10      Therefore, the BIST arrangement is confined to use in lower level tests where an external control of such initialization and source of test algorithm is available and thus represents a substantial inefficiency in utilization of chip space, as

15      alluded to above, even though the BIST arrangement is substantially essential to assure functionality of a chip and the board which includes it.

#### SUMMARY OF THE INVENTION

20      It is therefore an object of the present invention to provide an enhancement to a programmable memory BIST arrangement; expanding its utility to system level tests.

25      It is another object of the invention to provide an increase in efficiency of chip space utilization for BIST arrangements.

30      It is a further object of the invention to provide a default initialization capability for a programmable memory BIST arrangement to load a default set of desired test instructions if not provided by an external tester.

In order to accomplish these and other objects of the invention, an integrated circuit and an electronic system including an integrated circuit are provided, including a storage device for storing test instructions including an arrangement for receiving test instructions provided from an external tester, an arrangement for generating default test instructions, and an arrangement for supplying the default test instructions to the storage device for storing test instructions.

In accordance with another aspect of the invention, a method of performing system level testing of an electronic system is provided including steps of providing a system level test algorithm in a built-in self-test arrangement, transferring the system level test algorithm to an arrangement for storing a test algorithm, and operating the built-in self-test arrangement using the system level test algorithm.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a high-level block diagram of an exemplary architecture of a programmable memory BIST arrangement,

10           Figure 2 is a flow diagram illustrating  
initialization for manufacturing level and board  
level testing,

Figure 3 is a high-level block diagram illustrating a generalized overview of a programmable memory BIST architecture,

Figure 4 is a high level block diagram of the microcode based controller in accordance with the invention for a programmable memory BIST architecture such as that illustrated in Figure 1 or 3, and

Figure 5 is a flow chart illustrating the operation of the invention as an additional capability beyond that of Figure 2.

DETAILED DESCRIPTION OF A PREFERRED  
EMBODIMENT OF THE INVENTION

Referring now to the drawings, and more particularly to Figure 1, there is shown a high-level block diagram of an exemplary architecture of a programmable memory BIST module. (It should be understood that the depiction of Figures 1 - 3 are arranged to convey an understanding of the invention and are not admitted to be prior art as to the present invention.) Central to this architecture is a programmable memory BIST controller 10 which preferably includes a microcode based controller 100, an instruction store module 30 (both shown in Figure 3 and an instruction decode module 20.

The instruction decode module generates or controls generation of digital signals including data (40), address (50) and control (60) signal generators with which the memory under test is to be exercised. It is also generally desirable to provide for selection of a portion of memory to be tested (70) and selection of a port (80) through which test instructions may be loaded and responses to test signals are retrieved from the memory-under-test for analysis. Bi-directional communications are illustrated between controller 10 and signal generators and selectors 40 - 80 to indicate both control by the controller and the reporting of status of the respective generators and selectors and calls for next instructions. Unidirectional communications to the memory indicate that the BIST arrangement is principally concerned with the

exercising of the memory structure of interest and, while provisions for retrieval of signals from the memory responsive to the test procedure may be provided within the BIST arrangement, such  
5 arrangements are generally well-understood by those skilled in the art and need not be further discussed.

The development and initialization of manufacturing level and board level tests are  
10 illustrated in Figure 2. The process is begun (110) in the course of design of an integrated circuit including an embedded memory which must be designed to accommodate particular functions of the chip such as communications between functional elements as  
15 alluded to above. Assuming the memory structure to be of a new design for which suitable tests have not been previously developed, the memory test algorithm is generally approached as a description of a number of behaviors which the memory structure must be  
20 controlled to provide, as indicated at 115. This set of behaviors is then compiled into a list of supported instructions which will result in the generation of signals to be applied to the memory structure to cause those behaviors to be executed,  
25 as indicated at 120.

Generally, several tests will be developed to test the functionality of the chip and/or board at different points during manufacture or assembly. All or a plurality of these test algorithms are  
30 resident in memory of external test apparatus used as part of the manufacturing process or line and may be chosen at the will of an operator or automated,

as may be convenient or appropriate to a particular application. When a particular test procedure is chosen, the type of test procedure is determined at 125 to be either of the manufacturing level or board level test type.

If the test is of the manufacturing level type and the instruction store module of the BIST arrangement is of the register file type and scannable (as is assumed for purposes of this discussion), a scan loadable bit string of instructions is created at 130 and applied to the scan input, as indicated at 135. The bit string is then loaded as instructions by applying an appropriate number of scan clocks to the programmable memory BIST controller 10 to load the bit string into the instruction store module 30.

If, on the other hand, the test is of the board level type, a bit string in accordance with the IEEE 1149.1 standard is created, as indicated at 145, and an appropriate IEEE 1149.1 instruction is loaded into the instruction store module as instructions by applying an appropriate number of clock cycles, as indicated at 150. The bit string is then applied to the test data interface (TDI), as indicated at 155 and the test access port (TAP) controller is set to the SHIFT-DR state, as indicated at 160 and an appropriate number of clock cycles are applied to transfer the bit string into the instruction store module 30 as indicated at 160.

As was described above, in both manufacturing and board-level assembly tests, a bit string representing the selected memory test algorithm is

first loaded in the buffers of an external tester. By using the appropriate scan protocol, the external tester loads this bit string in the instruction store module. Therefore a programmable memory BIST 5 depends upon the availability on an external tester and therefore, in the absence of the present invention, cannot be used for system level testing where an external tester is not available to initialize the programmable memory BIST with the bit 10 string representing the test algorithm.

Referring now to Figures 3 and 4, the architecture of a programmable memory BIST arrangement which is also useable for system level testing will now be explained. The architecture of 15 a programmable memory BIST architecture as illustrated in Figure 1 and particularly the programmable memory BIST controller 10 can also be conceptualized as shown in Figure 3, comprising primarily a microcode-based controller 100 and an instruction decode module. The controller 100 provides instructions to the instruction decoder 20 module 20 and receives status signals and next instruction requests therefrom. The instruction decode module, in turn, communicates with specific 25 signal generators and/or registers which supply test signal patterns and sequences to the memory structure under test. The microcode-based controller 100 also receives test instructions for tester initialization, status signals and control 30 signals from an external tester or an associated circuit such as a power-up state detector.

As discussed above in regard to Figure 1, controller 100 also includes an instruction store module 30 and, in accordance with the invention, an instruction storage controller 200 which receives 5 the test instructions and control and status signals from an external tester or other associated circuit as alluded to above. Further, in accordance with the invention, an initialization storage module 210 is also provided as an input to instruction storage 10 controller 210.

A principal function of the instruction storage controller 200 is to provide an activation signal 220 to the initialization storage module 210 when a test procedure is called but no test instructions 15 are made available from an external tester. Upon receipt of such an activation signal 220, the initialization storage module provides default test instructions and status signals (e.g. to indicate completion of read-out) to the storage controller 210. Clock signals may also be provided by the 20 initialization storage module, if desired or not otherwise available.

It is preferred that the default test 25 instructions stored in the initialization storage module 210 be directed to system level tests but there is no technical necessity for such a limited application of the invention. That is, any desired test can be stored and supplied as a default test for storage in the instruction store module 30 of the programmable memory BIST controller 10 from 30 which the test procedure can be executed in the normal manner. Further, by virtue of the transfer

of the default test instructions from the initialization storage module 210 to the instruction store module 30, the facility for loading instructions for a particular test of either the 5 manufacturing level type or the board level type is unaffected by the inclusion of the invention in the programmable memory BIST controller, as is particularly evident from Figure 5.

Figure 5 illustrates the operation of 10 initialization in accordance with the invention. It will be appreciated that, with the exception of 125', steps 110 - 165 are the same as those shown in Figure 2 and discussed above. In the preferred form 15 of the invention illustrated in Figure 5, however, the determination of the type of test discriminates between three possibilities: manufacturing level, board level and system level. Manufacturing level and board level test discrimination is unaffected.

In the preferred embodiment of the invention, 20 the system level tests may be discriminated by the absence of instructions from an external tester. However, other techniques such as discrimination of 25 a source of a test command or a particular test command, itself could be used and could call for transfer of instructions from a selected initialization storage module 210 if more than one such initialization storage module is provided. The only limit on the number of types of tests which could be selectively supplied as defaults is the 30 number of conditions which can be readily discriminated and the amount of chip area which can be considered as efficiently allocated to storage or

other hardware for generation of instructions for different system or other level tests for which an external tester cannot readily be used.

When a test is called and it is determined that 5 test instructions are not available from an external tester, the initialization storage module is activated by signal 220, as discussed above and illustrated at 310 of Figure 5. When activated, the initialization storage module 210 generates and 10 loads default test instructions to the instruction store module 30 of programmable memory BIST controller 10, as shown at 320 of Figure 5. However, when test instructions are, in fact, available, the initialization storage module is not activated and 15 board level or manufacturing level test instructions are loaded in the normal fashion.

In view of the foregoing, it is seen that the invention provides additional utility and functionality for a built-in self-test arrangement 20 and thus improves efficiency of chip space usage and allocation. The invention allows full flexibility of programming of a programmable memory BIST arrangement while allowing additional desired testing to be performed independent of an external 25 tester such as system level tests after the chip with an embedded memory and/or board including such a chip has been placed in service.

While the invention has been described in terms 30 of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

## CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

1. An integrated circuit including an embedded memory and a built-in self-test arrangement including
  - 4 means for storing test instructions including
  - 5 means for receiving test instructions provided from
  - 6 an external tester,
  - 7 means for generating default test instructions,
  - 8 and
  - 9 means for supplying said default test
  - 10 instructions to said means for storing test
  - 11 instructions.
1. An integrated circuit as recited in claim 1, wherein said means for generating default test instructions includes an initialization storage means.
1. An integrated circuit as recited in claim 2, wherein said initialization storage means is a storage initialization module.

1       4. An integrated circuit as recited in claim 1,  
2 further including

3           means for activating said means for generating  
4 said default test instructions responsive to an  
5 absence of test instructions from an external  
6 tester.

1       5. An integrated circuit as recited in claim 1,  
2 further including

3           means for controlling a test operation, wherein  
4 said means for controlling a test operation includes  
5 means for supplying a control signal to an  
6 instruction storage controller and further includes  
7 said means for storing said test instructions.

1       6. An integrated circuit as received in claim 5,  
2 further including

3           means for activating said means for generating  
4 said default test instructions when only said  
5 control signal is supplied to said instruction  
6 storage controller.

1       7. An integrated circuit as recited in claim 1,  
2 wherein said means for generating default test  
3 instructions includes a memory for storing said  
4 default test instructions.

1       8. An electronic system including an integrated  
2       circuit having a built-in self-test arrangement  
3       therein, said integrated circuit including  
4           means for storing test instructions including  
5           means for receiving test instructions provided from  
6           an external tester,  
7           means for generating default test instructions,  
8       and  
9           means for supplying said default test  
10       instructions to said means for storing test  
11       instructions.

1       9. A system as recited in claim 8, wherein said  
2       means for generating default test instructions  
3       includes an initialization storage means.

1       10. A system as recited in claim 9, wherein said  
2       initialization storage means is a storage  
3       initialization module.

1       11. A system as recited in claim 8, further  
2       including  
3           means for activating said means for generating  
4           said default test instructions responsive to an  
5           absence of test instructions from an external  
6           tester.

1       12. A system as recited in claim 8, further  
2       including

3           means for controlling a test operation, wherein  
4       said means for controlling a test operation includes  
5       means for supplying a control signal to an  
6       instruction storage controller and further includes  
7       said means for storing said test instructions.

1       13. A system as recited in claim 12, further  
2       including

3           means for activating said means for generating  
4       said default test instructions when only said  
5       control signal is supplied to said instruction  
6       storage controller.

1       14. A system as recited in claim 12, wherein said  
2       control signal is supplied from an external tester.

1       15. A system as recited in claim 12, wherein said  
2       control signal is supplied from within said system.

1       16. A system as recited in claim 8, wherein said  
2       means for generating default test instructions  
3       includes a memory for storing said default test  
4       instructions.

1       17. A method of performing system level tests on an  
2       electronic system including an integrated circuit  
3       having a built-in self-test (BIST) arrangement  
4       therein for performing manufacturing level and board  
5       level testing and including means for storing a test  
6       algorithm, said method comprising steps of  
7           providing a system level test algorithm from  
8       said BIST arrangement,  
9           transferring said system level test algorithm  
10      to said means for storing a test algorithm in said  
11      BIST arrangement, and  
12      operating said BIST arrangement using said  
13      system level test algorithm.

SYSTEM INITIALIZATION OF MICROCODE-BASED  
MEMORY BUILT-IN SELF-TEST

ABSTRACT OF THE DISCLOSURE

The functionality of a programmable memory built-in self-test (BIST) arrangement for testing an embedded memory structure of an integrated circuit is extended to system level testing to ascertain 5 operability of the system after the integrated circuits and boards including them have been placed in service in larger systems, by generating default test signals which are loaded in an instruction store module when test instructions are not provided from an external tester. This additional utility of 10 the BIST arrangement, increases efficiency of chip space utilization and improves the system level test. Loading of test instructions from an external tester during chip manufacture and/or board assembly 15 is unaffected.

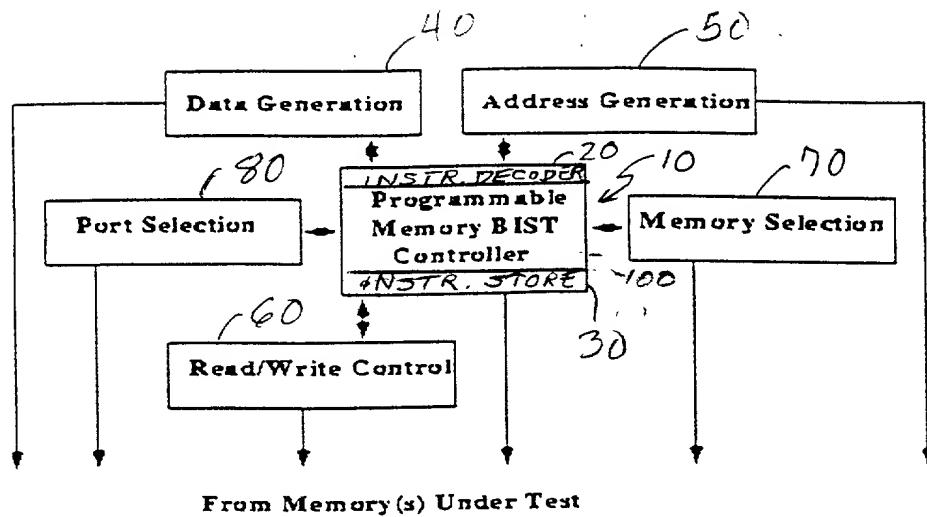


Figure 1. High Level View of a Programmable Memory BIST Module

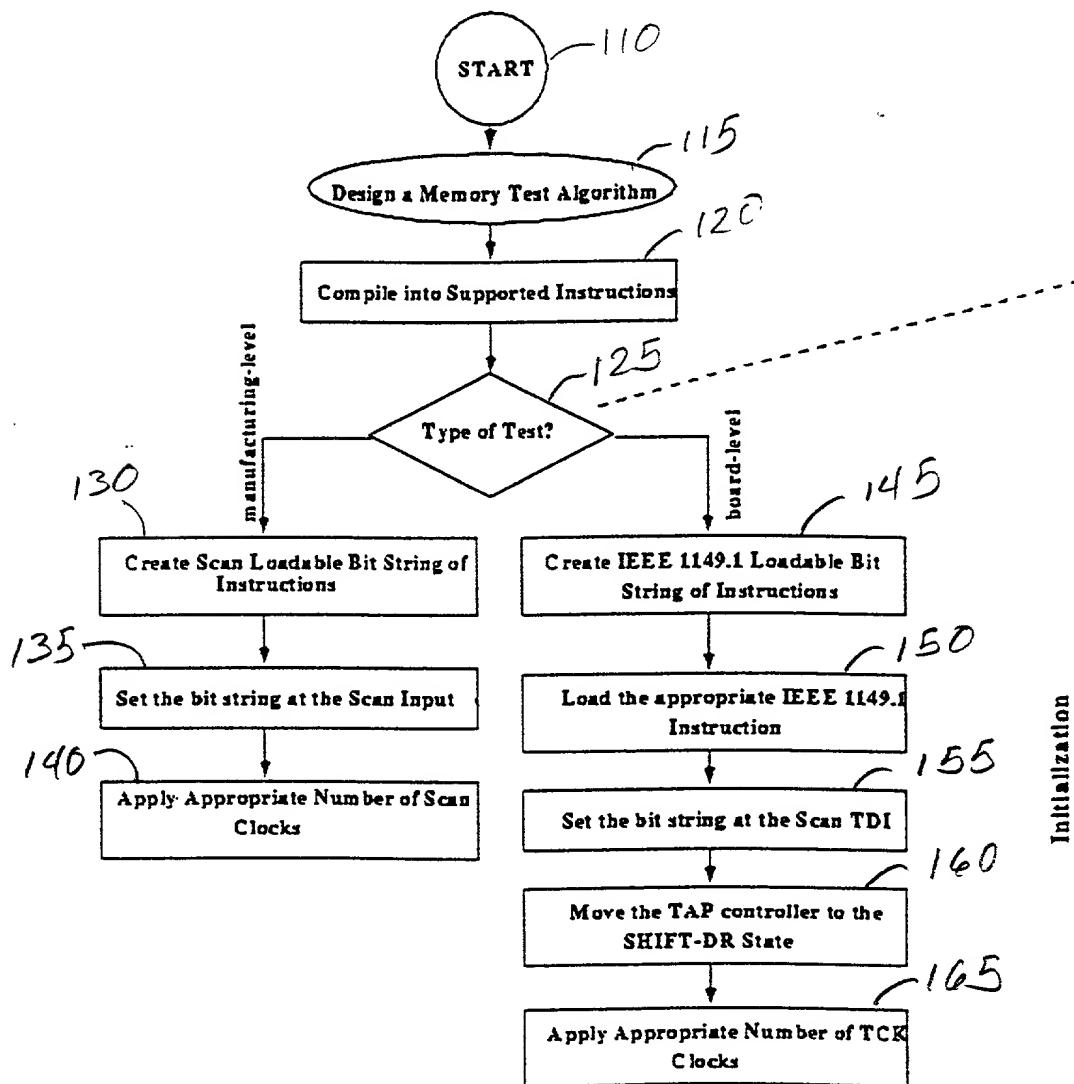


Figure 2. Initialization of Programmable Memory BIST Architecture in Manufacturing-level and Board-level Test

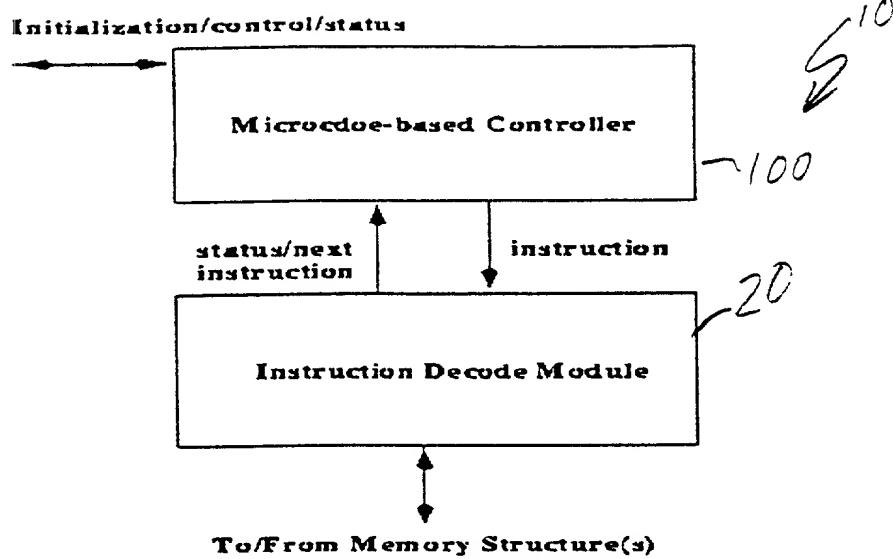


Figure 3. Overview of Programmable Memory BIST Architecture

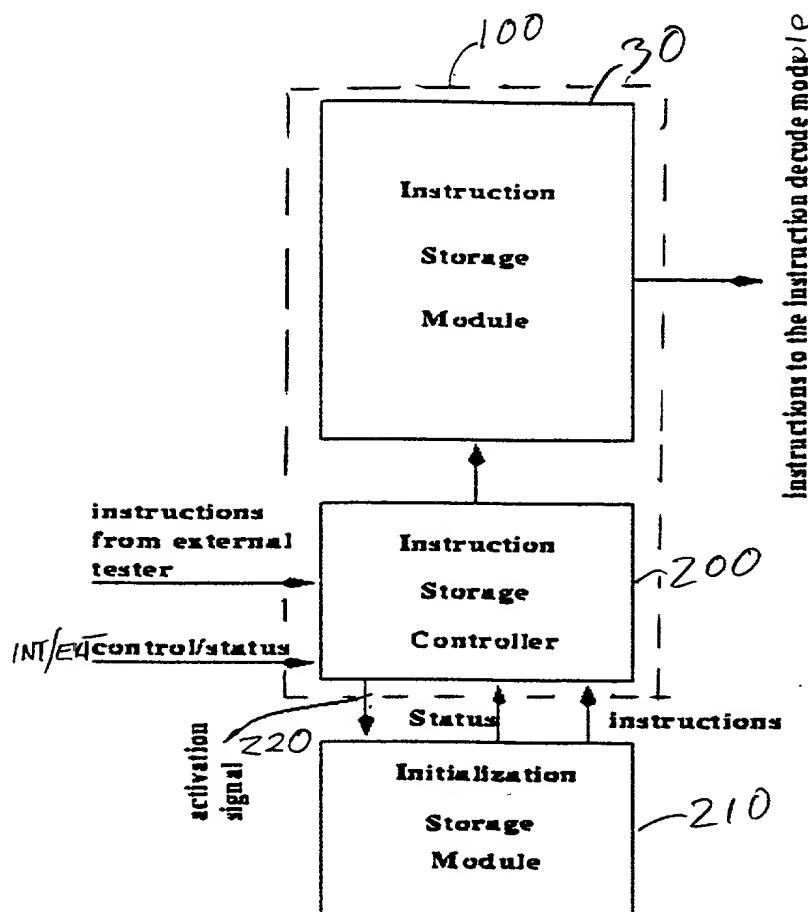


Figure 4. Microcode-based Controller for Programmable Memory BIST Architectures

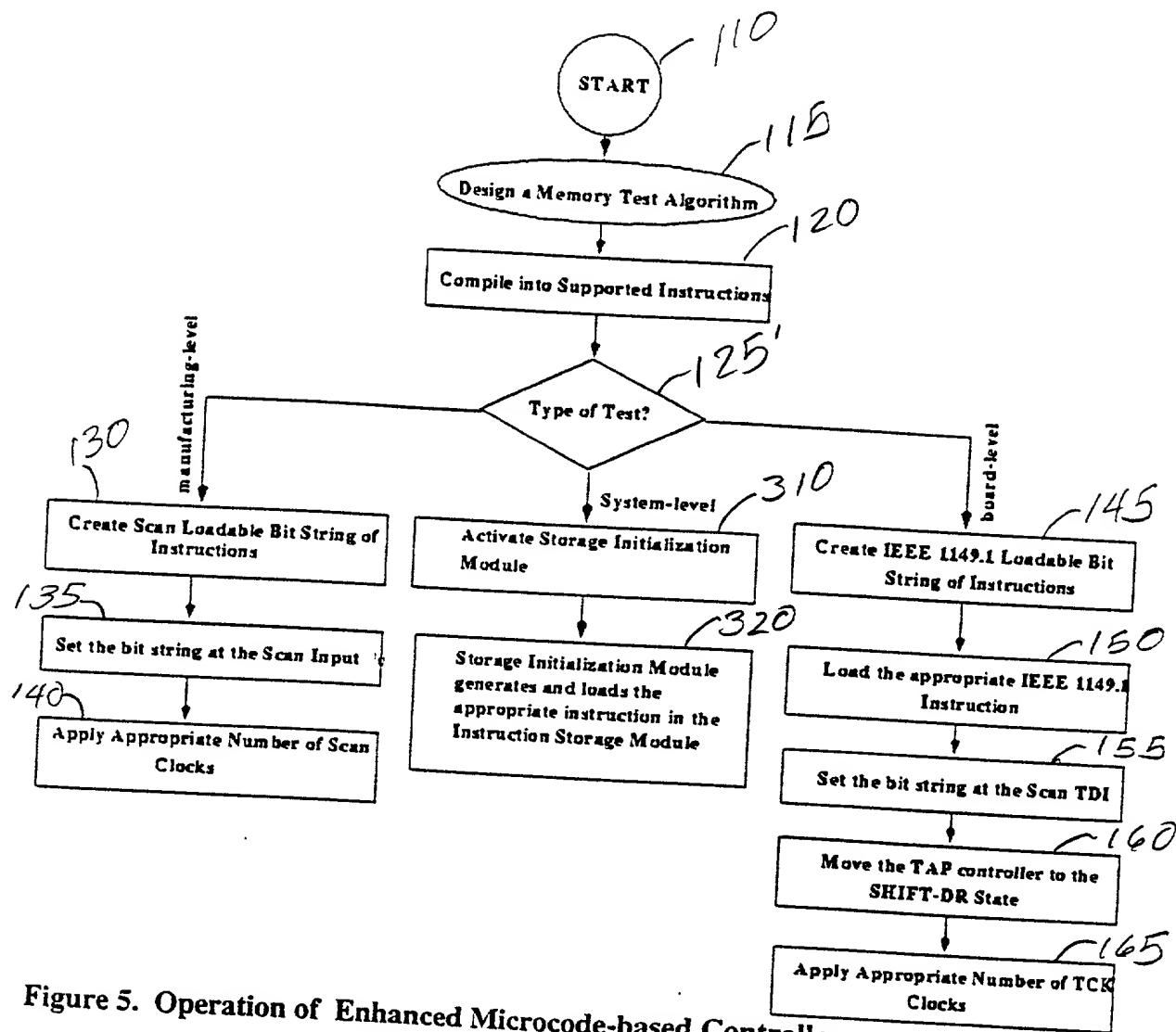


Figure 5. Operation of Enhanced Microcode-based Controller

## Application for United States Patent

## Declaration and Power of Attorney

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled **SYSTEM INITIALIZATION OF MICROCODE-BASED MEMORY BUILT-IN SELF-TEST** the specification of which:

(check one)  is attached hereto  
 was filed on \_\_\_\_\_ as  
 Application Serial No. \_\_\_\_\_  
 and was amended on \_\_\_\_\_ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).\*

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

## Prior Foreign Application(s)

## Priority Claimed

None (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	yes	no
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	yes	no

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

None (Application Serial No.)	_____ (Filing Date)	_____ (Status: patented, pending, abandoned)
----------------------------------	------------------------	---

Power of Attorney: As a named inventor, I hereby appoint Joseph P. Abate, Reg. No. 30,238, Aziz M. Ahsan, Reg. No. 32,100, Jay H. Anderson, Reg. No. 38,371, Ira D. Blecker, Reg. No. 29,894, Steven Capella, Reg. No. 33,086, T. Rao Coca, Reg. No. 29,784, Harold Huberfeld, Reg. No. 26,665, Todd M. C. Li, Reg. No. 45,554, Susan Murray, Reg. No. 38,252, Daryl K. Neff, Reg. No. 38,253, Eric W. Petraske, Reg. No. 28,459, Marc D. Schechter, Reg. No. 28,989, H. Daniel Schnurmann, Reg. No. 35,791, William P. Skladony, Reg. No. 33,787, Bernard Tiegerman, Reg. No. 29,707, Tiffany Townsend, Reg. No. 43,199, Christopher A. Hughes, Reg. No. 26,914, Edward A. Pennington, Reg. No. 32,588, John E. Hoel, Reg. No. 26,279, Joseph C. Redmond, Jr., Reg. No. 18,753, C. Lamont Whitham, Reg. No. 22,424, Marshall M. Curtis, Reg. No. 33,138, Michael E. Whitham, Reg. No. 32,635 and Joseph M. Martinez de Andino, Reg. No. 37,178, as attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. All correspondence should be directed to McGuireWoods LLP, 1750 Tysons Boulevard, Suite 1800, Tysons Corner, McLean, Virginia 22102-3915. Telephone calls should be directed to McGuireWoods, LLP at (703) 391-2510.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Title 37, Code of Federal Regulations, §1.56(a):

(a) A duty of candor and good faith toward the Patent and Trademark Office rests on the inventor, on each attorney or agent who prepares or prosecutes the application and on every other individual who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application. All such individuals have a duty to disclose to the Office information they are aware of which is material to the examination of the application. Such information is material where there is substantial likelihood that a reasonable examiner would consider it important in deciding whether to allow the application to issue as a patent. The duty is commensurate with the degree of involvement in the preparation or prosecution of the application.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and (1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability; or (2) it refutes, or is inconsistent with, a position the applicant takes in: (i) opposing an argument of unpatentability relied on by the Office, or (ii) asserting an argument of patentability.